GX8005 Datasheet

High performance, Low-Power AI Voice Recognition Processor

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Document Revision History:

Version	Date	Change Log	Author
V1.0	2025.03.20	Initial version	
V1.1	2025.06.24	Fix typo in “Input Low Level (VIL)” line for Table 5-1. Modify the note of “4.7 Power Management”.	chenzhd

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1.Features

GX8005 is a high-performance, cost-optimized voice recognition and processing chip. It integrates a low-power Neural Processing Unit (NPU) , a 32-bit RISC-V CPU, ADC/DAC, and comprehensive peripheral suite.
The chip is capable of voice signal processing and offline voice recognition. It is an ideal solution for various AI-voice interaction applications due to its ease of use and performance.

CPU:

- 32-bit RISC-V CPU with Digital Signal Processor(DSP) and Floating-Point Unit(FPU) extensions
- 8KB I-Cache, 4KB D-Cache
- Maximum frequency 200MHz
- Supports various audio encoding and decoding

NPU:

- Integrated neural processor gxNPU V122, maximum operation frequency: 200MHz
- Supports 8/16-bit quantization and weights compression
- Supports Deep Neural Network(DNN), Convolutional Neural Network(CNN), Long Short-Term Memory(LSTM) and other popular neural network architectures
- Compilers support TensorFlow and PyTorch

Memory:

- Built-in SRAM, size 176KB
- System in Package(SIP) Quad Serial Peripheral Interface(QSPI) Nor Flash, size 1MB，maximum frequency 100MHz
- 256-bit One-Time Programmable(OTP) memory
- Supports external Pseudo Static Random Access Memory(PSRAM)

Audio ADC:

- Integrated 1 channel 16-bit audio ADC
- Integrated PGA, supports 20~32dB gain with 2dB per step

Audio Out:

- Integrated high-performance audio output pipeline and DAC
- Integrated Class-D Power Amplifier (PA) delivering 1W output power at 5V into 8Ω / 4Ω load

Communication Interfaces:

- 2 Universal Asynchronous Receiver/Transmitter(UART) interfaces
- 1 I2C master and slave
- 4 Pulse Width Modulation(PWM) output ports

- 5V-tolerant General Purpose Inputs/Outputs(GPIOs)(P2 & P3)
- 6 Timers and watch dog timer

System Control:

- Integrated Power-On Reset(POR) and Brown-Out Reset(BOR)
- Internal 12MHz OSC and PLL
- No external crystal clock required

Voltage Supply:

- Single power 3.0~5.5V supply
- Integrates Low Dropout Regulators(LDOs) for core and IO power supply

Package Type:

- SOP-8

Quality:

- Temperature: -40~85℃

2.Chip Architecture

2.1.Block Diagram

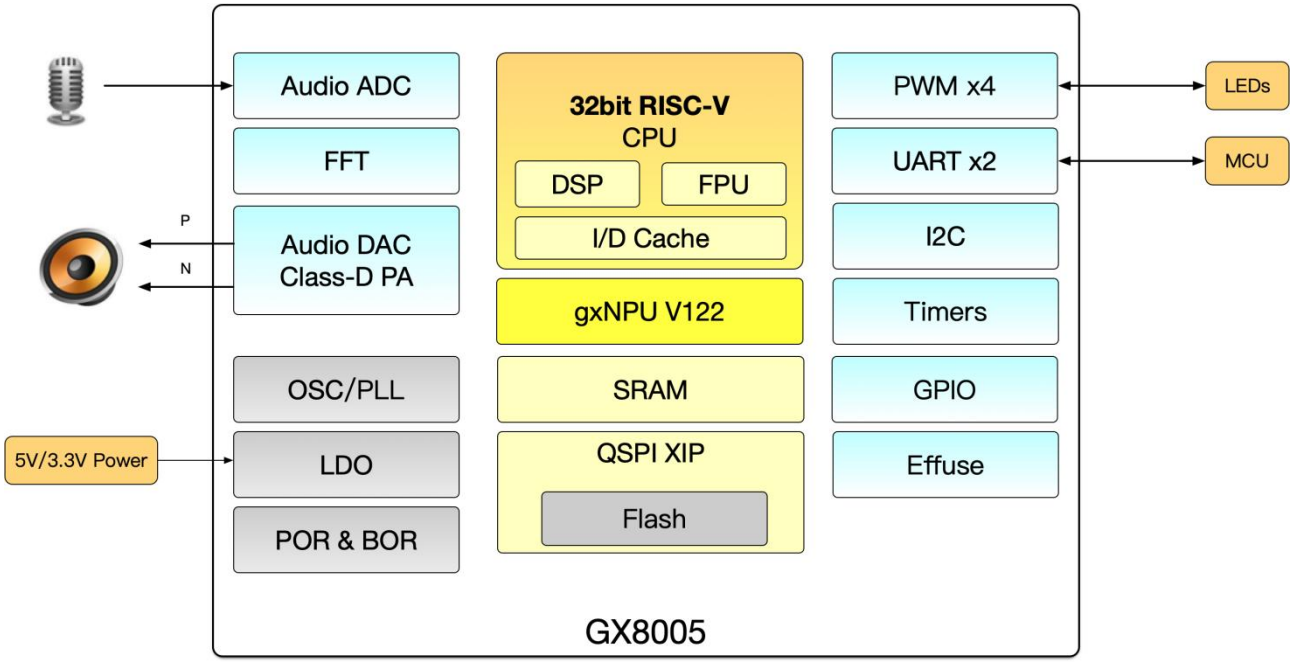


Figure 2- 1 GX8005 chip block diagram

3.Pin Description

3.1.Pin Map

GX8005 is available in 8-pin SOP-8 package.

Figure 3- 1 GX8005 pin map

3.2.Pins description

Table 3- 1 Pins description

Pin Num	Pin Name	Type	Domain	Description
1	VDDIO	Power		Digital IO power output, range 2.85~3.3V, max current 200mA,external capacitor required.
2	P3	Digital	VDDIO	MPIO P3，5V tolerant and supports open-drain to 5V with externally pull-up resistor
3	P2	Digital	VDDIO	MPIO P2，5V tolerant and supports open-drain to 5V with externally pull-up resistor
4	ADC0/BOOT	Analog/Digital	AVDD25	Analog input of audio ADC0, share with BOOT. *Note: During the boot stage, if the BOOT pin is pulled LOW, the device will automatically enter Flash Programming Mode
5	GND	Ground		GND
6	P1/PA_P	Analog/Digital	VCC5	MPIO P1(IO power from VCC5) and audio PA_P output，and supports open-drain to 3.3V with external pull-up resistor
7	VCC5	Power		DC5V INPUT
8	P0/PA_N	Analog/Digital	VCC5	MPIO P0(IO power from VCC5) and audio PA_N output，and supports open-drain to 3.3V with external pull-up resistor

3.3.GPIO Pin Multiplexing Functions

Table 3- 2 Pin Multiplexing Functions

Pin	Pin Name	Function00	Function01	Function02	Function03	Function04	Function05	Function06	Function07
2	P3	IDLE with pull-up		UART0_TX	PWM3	JTAG_TCK	I2C_SCL		GPIO3
3	P2	IDLE with pull-up		UART0_RX	PWM2	JTAG_TMS	I2C_SDA		GPIO2
4	ADC0/BOOT	BOOT							
6	P1/PA_P	**IDLE**	PA_P	UART1_RX	PWM1		I2C_SCL	DAC_N	GPIO1
8	P0/PA_N	**IDLE**	PA_N	UART1_TX	PWM0		I2C_SDA	DAC_P	GPIO0

Note: **IDLE**: High impedance, no function

4.Function Overview

4.1.CPU Architecture

- 32-bit RISC-V CPU, maximum frequency 200MHz
- 8KB I-Cache，4KB D-Cache
- Supports DSP and FPU acceleration unit

4.2.Memory

- Integrated 176KB SRAM
- Internally encapsulates 1MB SPI NOR flash in SIP style
  - Supports standard, dual or quad mode of SPI interface
  - Allow to XIP directly from flash
  - SPI clock frequency up to 100MHz

4.3.Clock

- On-chip12MHz oscillator circuit
- One phase-locked loops (PLL)

4.4.NPU

- NationalChip's gxNPU V122
- Supports DNN/CNN/LSTM and other popular neural network architectures
- Supports 8/16 bit quantization, and weights compression
- Compilers support direct conversion from TensorFlow and PyTorch

4.5.Audio

- Integrated single channel 16-bit audio ADC, supports sample rate of 16KHz
- Integrated PGA, supports 20~32dB gain with 2dB per step
- Integrated high-performance audio output pipeline and DAC
- Integrated Class-D PA delivering 1W output power at 5V into 8Ω / 4Ω load

4.6.System Peripheral

- I2C
  - Integrated one I2C controller
  - Master or Slave Mode
  - Supports speed 100KHz，400KHz and up to **1MHz (P2 & P3 port only, with VDDIO = 3V)**

- DMA
  - 3 channel DMA
  - Supports 8/16/32-bit data width
  - Supports memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfer types

- UART
  - Integrates 2 UART interfaces
  - Full-duplex operation
  - Supports speed up to 1.5 Mbps

- Timer
  - Consists of six 32-bit up-counters
  - Integrated RTC timers

- WDT
  - Programmable and hard coded reset pulse length
  - An interrupt is generated first, and if the interrupt is not cleared by the service routine before the second timeout, a system reset is generated
  - 32-bit Watchdog Timer(WDT) counter

4.7.Power Management

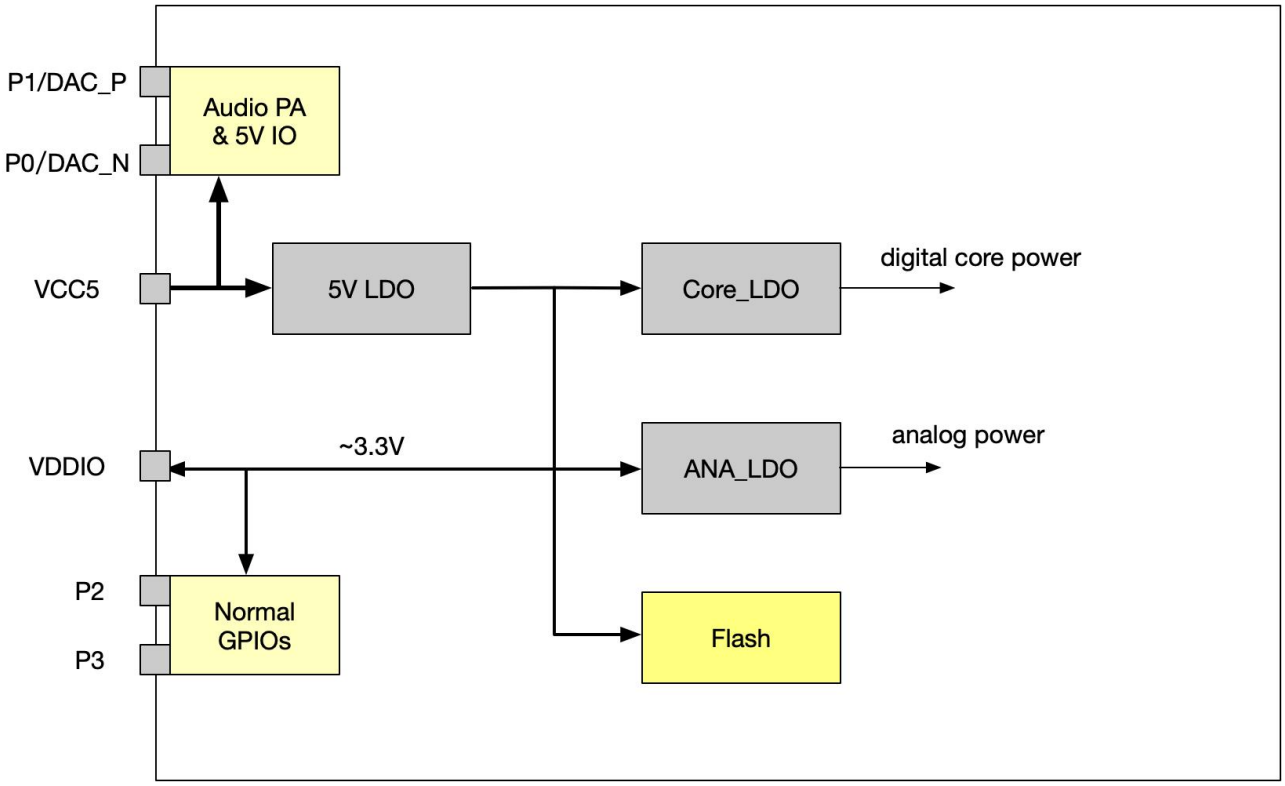


Figure 4- 1 Chip power supply system

- VCC 5V input range: 3.0V~5.5V [1]
- VDD IO output range: 2.7V~3.3V

1*,*Note:

①. When VCC5=[3.6V~5.5V]，LDOIO must be in work mode, and VDDIO can be configured to 3V/3.3V. It is strongly recommended that the VCC5 power input (including ripple) always maintains a headroom of at least 150mV above the configured VDDIO output voltage. This is to ensure LDOIO can output stably.

②. When VCC5 = [3.3V ~ 3.6V), LDOIO must be in work mode, and VDDIO can only be configured to 3V output. However, if the valley (lowest point) of the VCC5 ripple falls below 3.15V, it may trigger LDOIO to automatically enter bypass mode. After that, VDDIO will equal VCC5. It is strongly recommended that the VCC5 power input (including ripple) always maintains a headroom of at least 150mV above the configured VDDIO output voltage. This is to ensure LDOIO can output stably.

③. When VCC5 = [3.0V ~ 3.3V), considering potential ripple, it is strongly recommended to configure LDOIO into bypass mode to avoid repeated toggling between work mode and bypass mode. In this state, VDDIO = VCC5.

4.8.POR and BOR

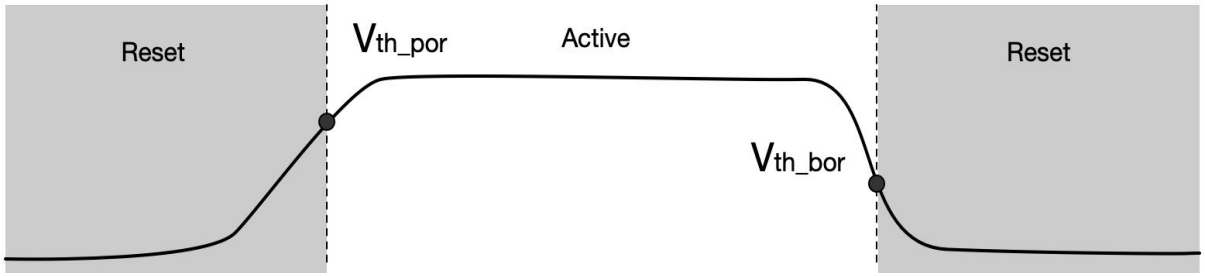


Figure 4- 2 Power on reset and brown out reset

Table 4-1 POR and BOR threshold

Parameter	Description	Min	Typ	Max	Unit
Vth_por	VCC5 voltage > Vth_por, reset release.	2.6	2.8	3.0	V
Vth_bor	VCC5 voltage < Vth bor, will enter reset mode.	2.4	2.6	2.8	V

5.Applications

5.1.Typical Applications

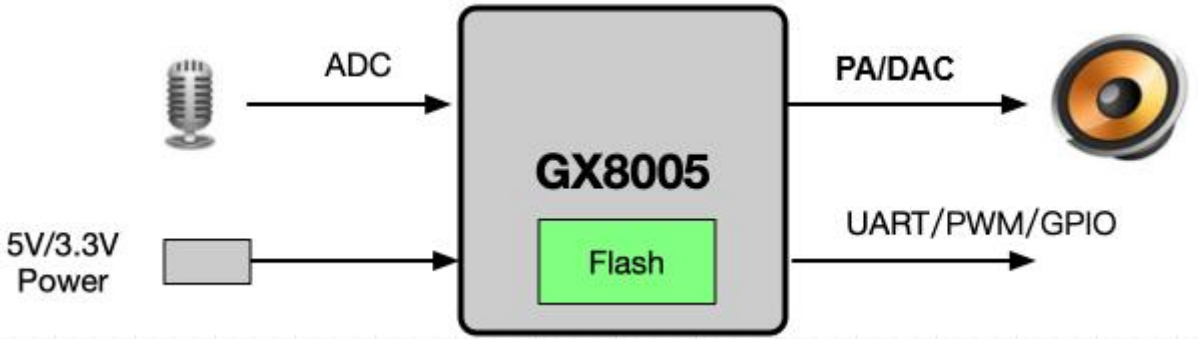


Figure 5- 1 Block diagram of voice enabled IOT device

Key Features:

- Single Analog microphone input.
- Direct connect to speaker with Class-D PA delivering 1W output power at 5V into 8Ω / 4Ω load
- Single power supply from 3.0V to 5.5V
- 5V tolerate IO to external MCU
- AI voice recognition, voice key word detection, voice commands recognition

5.2.Recommended Operating Condition

Table 5- 1 Recommended operating conditions

Parameters	Min	Typ	Max	Unit
Power supply voltage(VCC5)	3.0	5	5.5	V
IO Power output Voltage(VDD_IO)	2.7	3	3.3	V
Output High Level (VOH) for P2 & P3	2.7	3	3.3	V
Output Low Level (VOL) for P2 & P3			0.4	V
Output High Level (VOH) for P0 & P1	3.6	5	5.5	V
Output Low Level (VOL) for P0 & P1		0	0.4	V
Input High Level (VIH)	2.0		5.5	V
Input Low Level (VIL)	-0.3		0.8	V
Pull-up Resistor, for P2 & P3	27K	40K	65K	Ω
Pull-down Resistor, for P2 & P3	33K		87K	Ω
Pull-up Resistor, for P0 & P1		6K		Ω
Pull-down Resistor, for P0 & P1		6K		Ω

Table 5- 2 Recommended operating conditions continue

Parameters	Min	Typ	Max	Unit	Remark
Storage Temperature	-40	25	150	℃	
Operating Ambient Temperature	-40	25	85	℃	

5.3.Electrostatic Discharge

Table 5- 3 Electrostatic discharge

Parameters	Min	Max	Unit
Human Body Model (HBM)	-4	4	kV
CDM	-1000	1000	V

6.Electronic Specification

6.1.ADC Characteristics

Table 6- 1 ADC performance testing report

＊all specifications at T= 25℃, VCC5= 5V, AVDD25= 2.5V, ADC_GAIN= 6dB, single-ended input

Parameter	Test condition	Min	Typ	Max	Unit
Input Common Mode	AVDD25/2	-	1.25	-	V
Pga_Gain		-	0~32	-	dB
Full Scale Input Voltage	(THD+N=0.2%)	-	2.47	-	Vpp
Noise	Fs=16KHz A-weighted	-	-81	-	dBFS
SNR	Fs=16KHz A-weighted	-	80	-	dB
Dynamic Range	4.4mVpp input (-60dB of max input level) Fs=16KHz A-weighted	-	78	-	dB
THD	Best at -6dBFS input Fs=16KHz A-weighted	-	-73	-	dB
Current	ADC+PGA+LDO	-	2.83	-	mA

6.2.DAC Characteristics

Table 6- 2 DAC performance testing report

＊all specifications at T= 25℃, VCC5= 5V

Parameter	Min	Typ	Max	Unit	Test condition
Output Swing	-	5.9	-	dBu	Input 0dBFs **Single ended mode**
	-	1.52	-	Vrms	
Noise	-	-63	-	dBu	
SNR	-	68.5	-	dB	
THD+N	-	-52.9	-	dB	
Output Swing	-	4.76	-	dBu	Input 0dBFs **Differential mode**
	-	1.34	-	Vrms	
Noise	-	-76	-	dBu	
SNR	-	81	-	dB	
THD+N	-	-53	-	dB	

6.3.PA Characteristics

Table 6- 3 PA performance testing report (RL = 8Ω)

＊all specifications at T= 25℃, VCC5= 5V，PA output load= 8Ω

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Power Voltage	VCC5		3	5	5.5	V
Quiescent Current	IDD	VIN=0V，VCC5 = 5V，No Load		19		mA
Sampling Frequency	Fsw	VCC5 = 3.0V to 5.25V		24.576		MHz
Output Power	PO	THD+N=1%，f=1KHz,VCC5=5V		1		W
		RL=8 Ω (VCC5 CAP=100uF)				
		THD+N=3%，f=1KHz,VCC5=5V		1		W
		RL=8 Ω (VCC5 CAP=1uF)				
		THD+N=10%，f=1KHz,VCC5=5V		1.15		W
		RL=8 Ω (VCC5 CAP=100uF)				
		THD+N=10%，f=1KHz,VCC5=5V		1.1		W
		RL=8 Ω (VCC5 CAP=1uF)				
Total Distortion+Noise	THD+N	VCC5=5V，f=1KHz	-	0.8		%
		RL=8 Ω，Po=0.5W (VCC5 CAP=100uF)				
		VCC5=5V，f=1KHz		1.3		%
		RL=8 Ω，Po=0.5W (VCC5 CAP=1uF)				

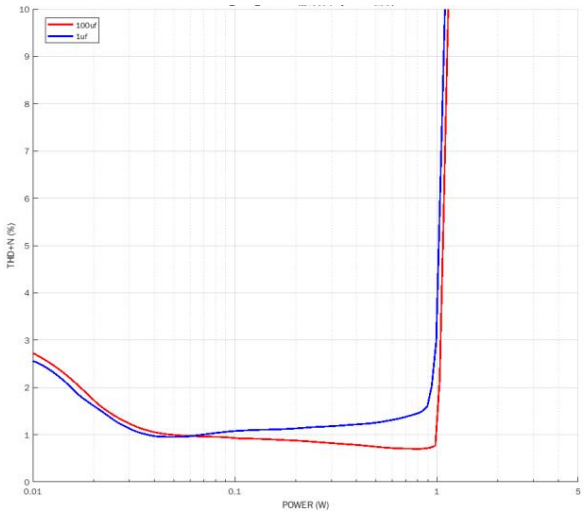


Figure 6- 1 THD+N vs Output Power (RL = 8 Ω)

Table 6-4 PA performance testing report (RL = 4Ω)

＊all specifications at T= 25℃, VCC5= 5V，PA output load= 4Ω

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Power Voltage	VCC5		3	5	5.5	V
Quiescent Current	IDD	VIN=0V，VCC5 = 5V，No Load		19		mA
Sampling Frequency	Fsw	VCC5 = 3.0V to 5.25V		24.576		MHz
Output Power	PO	THD+N=1.5%，f=1KHz,VCC5=5V		1		W
		RL=4 Ω (VCC5 CAP=100uF)				
		THD+N=1.5%，f=1KHz,VCC5=5V		1		W
		RL=4 Ω (VCC5 CAP=1uF)				
		THD+N=10%，f=1KHz,VCC5=5V		1.65		W
		RL=4 Ω (VCC5 CAP=100uF)				
		THD+N=10%，f=1KHz,VCC5=5V		1.65		W
		RL=4 Ω (VCC5 CAP=1uF)				
Total Distortion+Noise	THD+N	VCC5=5V，f=1KHz	-	1.3		%
		RL=4 Ω，Po=0.5W (VCC5 CAP=100uF)				
		VCC5=5V，f=1KHz		1.3		%
		RL=8 Ω，Po=0.5W (VCC5 CAP=1uF)				

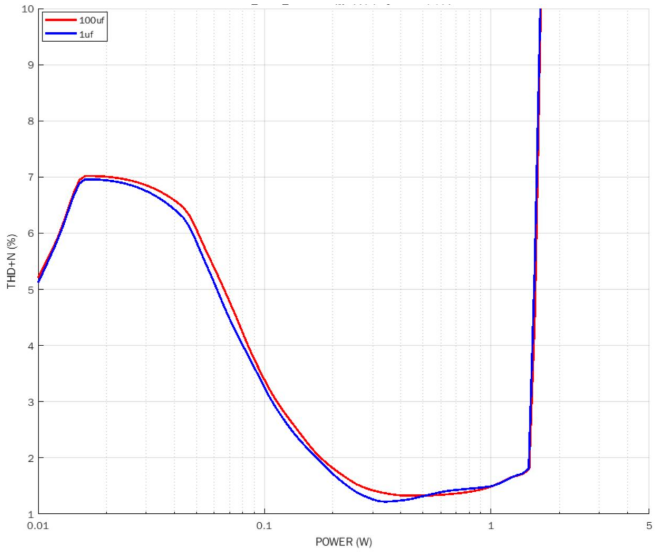


Figure 6-2 THD+N vs Output Power (RL = 4 Ω)

6.4.PMU Characteristics

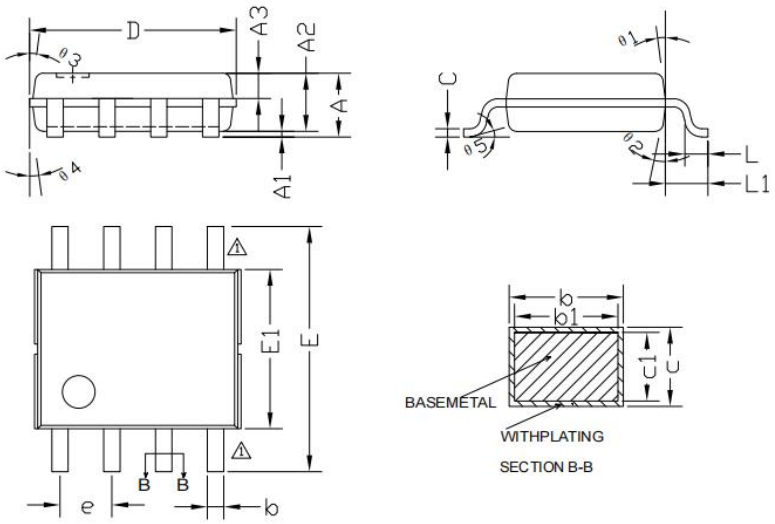
Table 6- 5 PMU performance testing report

＊all specifications at T= 25℃

Symbol	Description	Min	Typ	Max	Unit
VCC5 Input voltage	Input Voltage.PA Supply Voltage.P0&P1 IO Voltage	3.0	5	5.5	V
VDDIO Output Voltage	Internal LDO-IO output.IO Voltage(except P0 & P1).Analog supply voltage	2.7	3	3.3	V
VDDIO Output Current	Internal LDO-IO Loading current		200		mA

7.Package Information

7.1.Package Specification



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.65
A1	0.10	--	0.25
A2	1.40	1.42	1.50
A3	0.57	0.62	0.67
b	0.33	--	0.47
b1	0.32	0.41	0.44
c	0.20	--	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27(BSC)		
L	0.50	0.60	0.70
L1	1.05(BSC)		
θ1	6°	~	12°
θ2	6°	~	12°
θ3	5°	~	10°
θ4	5°	~	10°
θ5	0°	~	6°

Figure 7- 1 SOP-8 package specification

7.2.Chip Mark Description

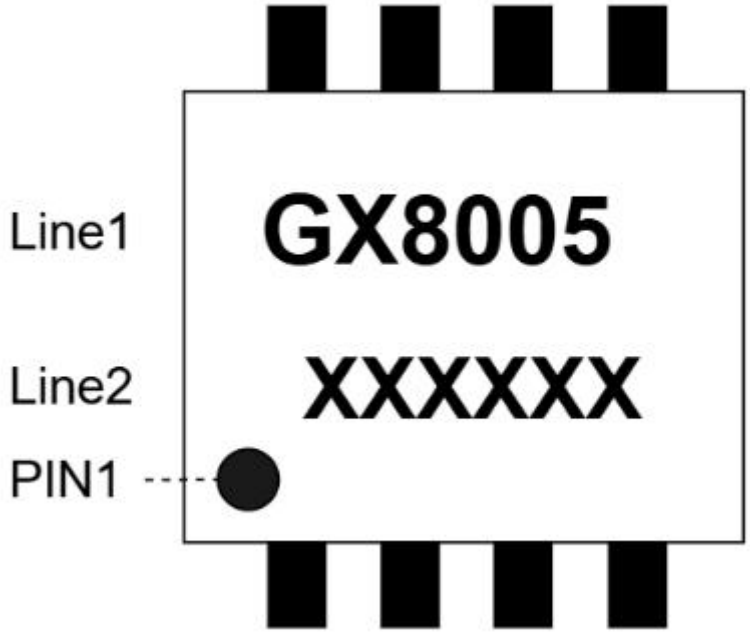


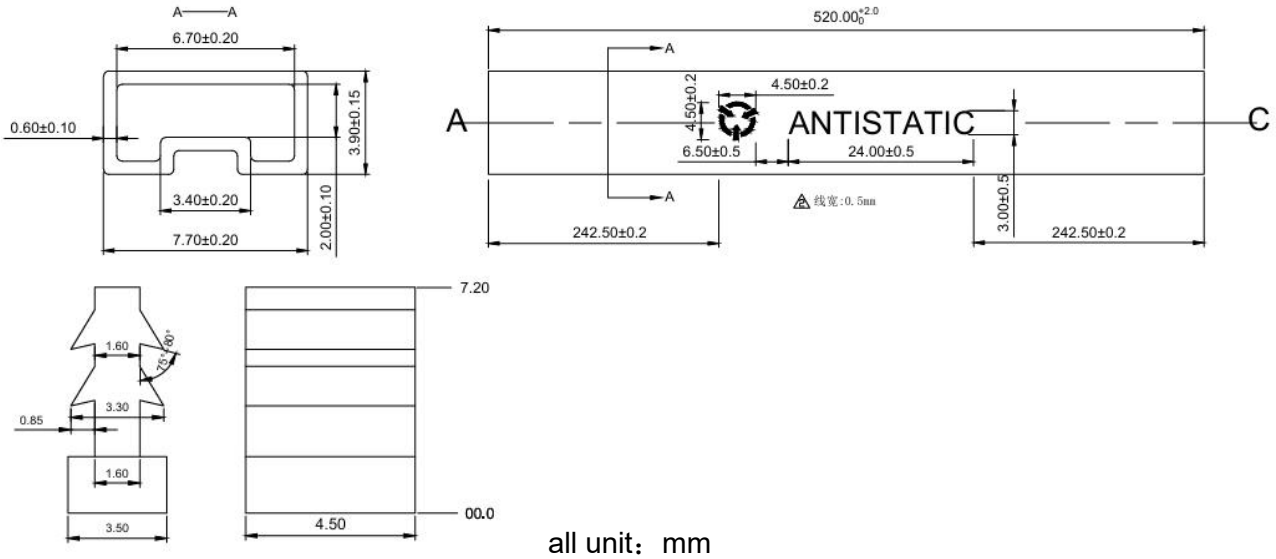
Figure 7- 2 Chip mark description

Description:

- Line 1: Chip name
- Line 2: 6 digit of production lot number
- PIN 1: Pin 1 start point mark

7.3.TUBE Specification

1.TUBE Information



all unit：mm

Figure 7-3 TUBE information

7.4.Convection Reflow Profile

The test results comply with three-stage reflow soldering requirements, with a reflow temperature of 260℃. The details are as follows:

Table 7- 1 Convection reflow profile

Profile Feature	Note	Pb-Free Assembly
Average ramp-up rate	T_{smax} to T_p	0.6~1.5℃/sec
Preheat	-Temperature Min(T_{smin})	150℃
	-Temperature Max(T_{smax})	200℃
	-Time(min to max)(ts)	60-120sec
Time maintained above:	-Temperature(T_L)	217℃
	-Time(t_L)	60-150 sec
Peak Temperature(Tp)		250±5℃
Time within 5℃ of actual Peak Temperature(tp)		≥30sec
Ramp-down Rate		≤3℃/ sec
Time 25℃ to Peak Temperature		≤8 min

8.Ordering Information

Table 8- 1 Ordering information

Ordering Code	Embedded SPI Nor Flash	Package	MOQ
GX8005A	1MByte	SOP-8	10k

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