1.PDM interface：

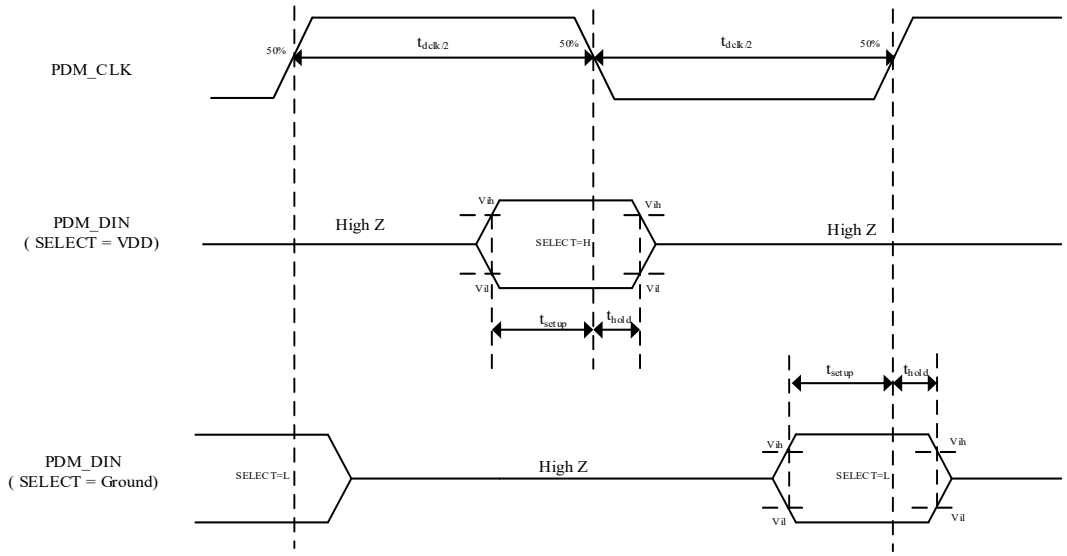

Figure 1- 1 PDM Timing Diagram

Parameter	Symbol	Min.	Typ.	Max.	Units
PDM clock period	t_{dclk}		976.6		ns
PDM clock duty cycle		48		52	t_{dclk}
PDM Data setup time	t_{setup}	17			ns
PDM Data hold time	t_{hold}	4			ns

Table 1- 1 PDM Timing Specification (master mode)

2. I2S interface：

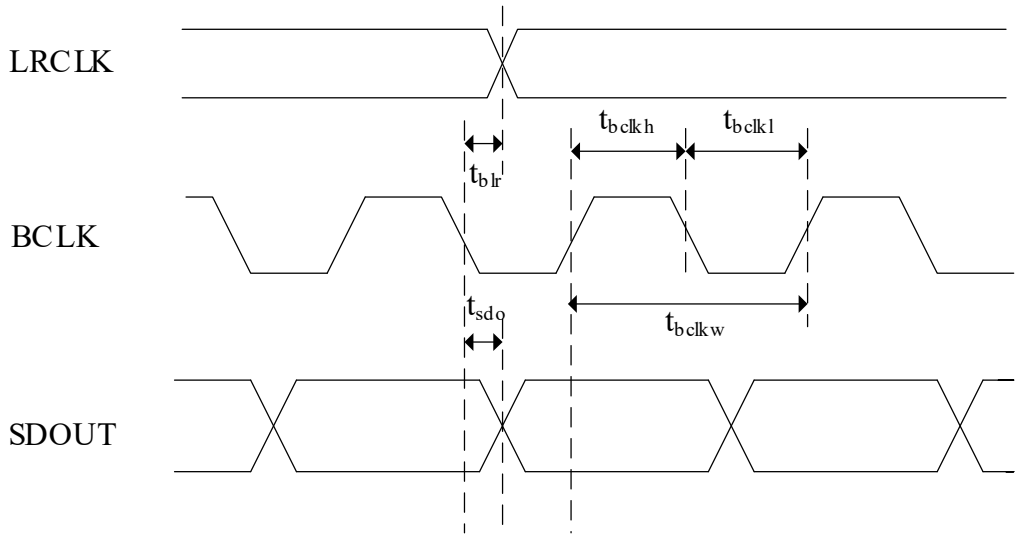

Figure 2- 1 Serial audio Timing Diagram

PARAMETER	Symbol	MIN	MAX	unit
MCLK frequency			24.576	MHz
MCLK duty cycle		40	60	%
LRCLK frequency			48	KHz
LRCLK duty cycle		40	60	%
BCLK frequency			3.072	MHz
BCLK pulse width low	T_{BCLKL}	100		ns
BCLK Pulse width high	T_{BCLKH}	100		ns
BCLK falling to LRCLK edge	T_{BLR}	-10	10	ns
BCLK falling to SDOUT valid	T_{SDO}		11	ns

Table 2-1 Serial audio timing Specification (Master mode)

3.I2C interface：

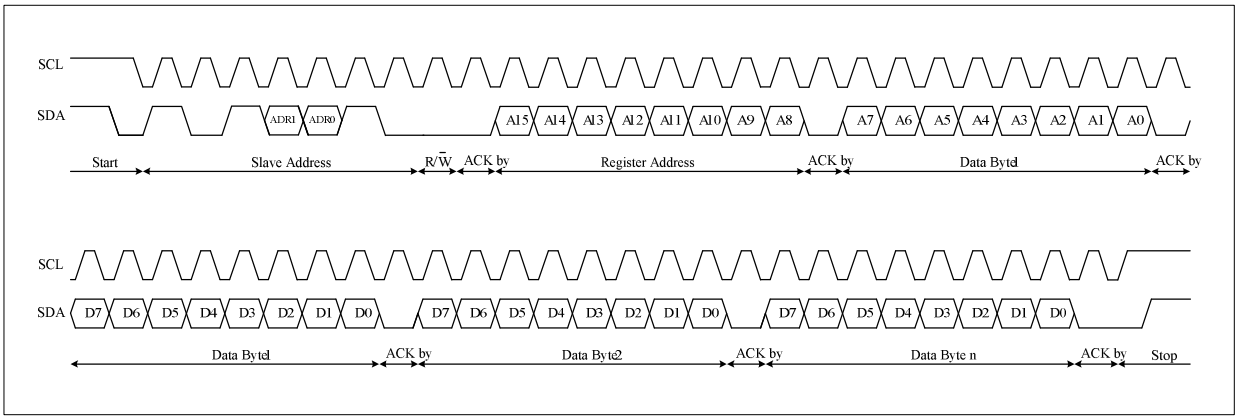

Figure 3-1 I2C Slave Write Operation

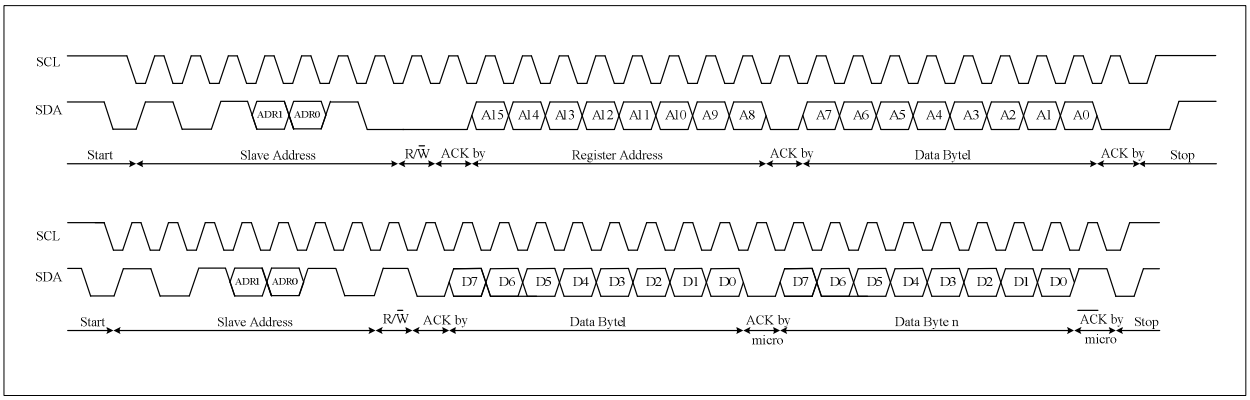

Figure 3- 2 I2C slave Read Operation

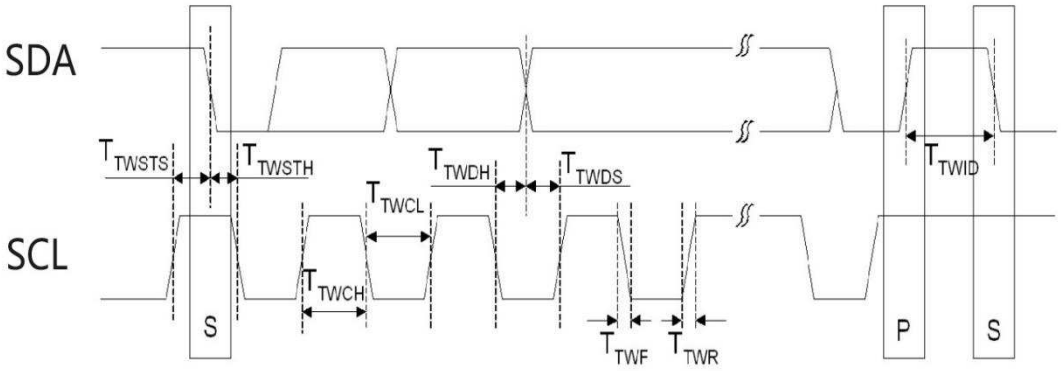

Figure 3-3 I2C Slave Timing Diagram

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	SCL		400	KHz
Bus Free Time Between Transmissions	TTWID	1.3		us
Start Condition Hold Time	TTWSTH	0.6		us
Clock Low time	TTWCL	1.3		us
Clock High Time	TTWCH	0.4		us
Setup Time for Repeated Start Condition	TTWSTS	0.6		us
SDA Hold Time from SCL Falling	TTWDH		900	ns
SDA Setup time to SCL Rising	TTWDS	100		ns
Rise Time of SCL	TTWR		300	ns
Fall Time SCL	TTWF		300	ns

Table 3- 1 I2C slave timing specification

4.SPI interface(slave)

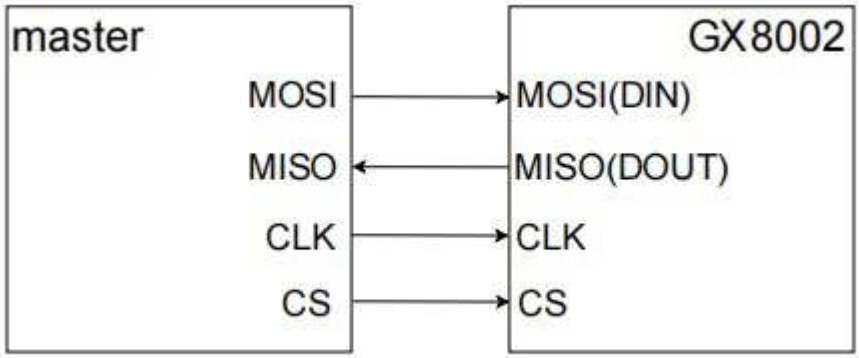

Figure 4- 1 SPI slave communication

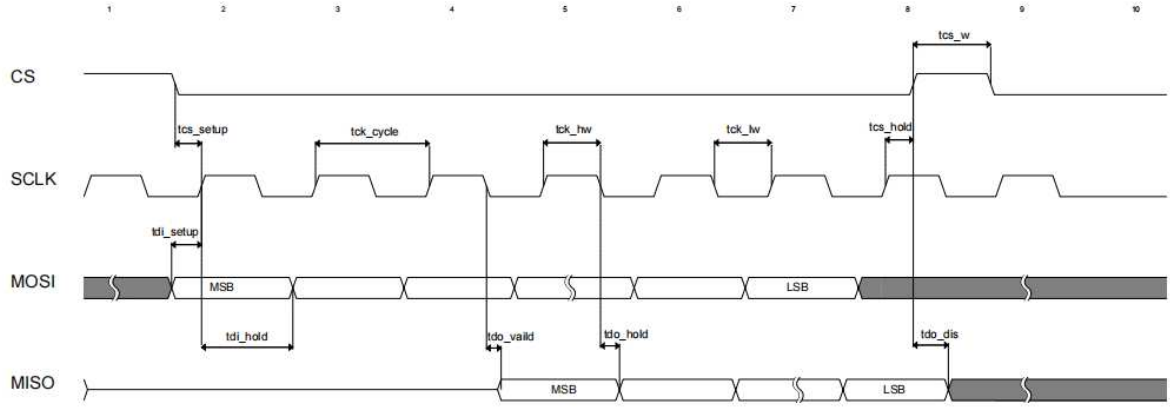

Figure 4- 2 SPI slave interface timing Diagram

Parameter	Symbol	Min	Max	Unit
tck_cycle	SPI clock cycle	500ns		
fck	SPI clock frequency		2MHz	MHz
tck_hw	SCLK high pulse width 0.4 * tck_cycle	200ns		ns
tck_lw	SCLK low pulse width 0.4 * tck_cycle	200ns		ns
tcs_setup	CS setup time	10ns		ns
tcs_hold	CS hold time	20ns		ns
tdi_setup	MOSI input setup time	10ns		ns
tdi_hold	MOSI input hold time	20ns		ns

tdo_hold	MISO output hold time	10ns		ns
tdo_valid	MISO valid output time	80ns		ns
tdo_dis	MISO output disable time		20ns	ns

Table 4-1 SPI slave timing specification